CDF Pixel Chip

Assume chip has a 18 x 160 array of pixels each 50 x 400 u.
Active area = 7.2 mm wide x 8.0 mm high.
Chip area with overhead for periphery logic = 7.4 x 11 mm = 81.4 mm^2.

Chips to be fabricated on 200 mm (8”) diameter wafers.
Wafer area = 31416 mm^2
Estimate 15% of area lost to edge, streets and PCMs.
Useable area = 26700 mm2

Chips/wafer = 26700/82 = 325
Assume 60% yield
Good chips/wafer = 195

Fabrication Costs and Schedule

First prototype using basic core and CDF periphery:

- 18 columns x 16 rows = 7.4 mm x 3.8 mm = 28.1 mm^2
- 30 mm2 x $1250/mm = $37500
- Design – 6 months
- Fabrication – 2.5 months
- Test - 2 months by designers and more by DAQ personnel

Second prototype

- $37500
- Design – 2 months
- Fabrication – 2.5 months
- Test – ???

Engineering run – full size chip (could be production if lucky)

- $161,000 for 10 wafers
- $31,700 for 10 more wafers
- Approximately 2000 good chips from 10 wafers
- Design – 2 months
- Fabrication – 2.5 months

Current R&D Plan

Complete testing of Pre-FPIX2_T

Test Pre-FPIX2_I in July and August

Submit FPIX2???? at the beginning of August.
Includes serial interface and programming DACs to reduce external component count and chip pad count.

Submit FPIX3 with DAQ interface for BTEV by April 1, 2001